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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 015

Application Number: 09/409,940
Filing Date: September 30, 1999
Appellant(s): BULLIS ET AL.

John A. Sawyer, Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 23 September 2003.

EXAMINER'S ANSWER

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct. However appellants have improperly introduced arguments and allusions related to patentability not related to the **status of the claims**.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments and final rejection contained in the brief is incorrect. Applicants filed an after final amendment (paper # 9) and declaration (paper # 10) on 27 May 2003. The examiner issued an Advisory Action (paper # 11) on 9 June 2003 stating the amendment has not been entered and that "the declaration merely expresses the opinion of the inventor, is not supported by sufficient evidence, and is in variance with the Inventor's previously filed declaration (paper #5)". (Please see paper #11)

(5) Summary of Invention

The summary of invention contained in the brief is agreed with.

(6) Issues

The examiner has applied 35 USC 112(1) rejections to claims 1-23 for lack of enablement of claimed features relating to the terms interface, snooper, checker, and generator. Appellants filed a First Declaration (paper #5) under 37 CFR 1.132 in response to the first office action (paper # 3). The examiner objected to the First Declaration as containing new matter and indicated that the information (new matter) contained in the First Declaration should have been incorporated into the specification to provide enablement for the claims. (please see paper #7) Appellants subsequently filed a Second Declaration (paper # 10 - after final) without the new matter but based solely on the opinion of the inventor that one skilled in the art would know how to make and/or use the invention.

Appellants now rely on statements made based on the opinion of the inventor contained in a Second Declaration (paper # 10) to support arguments relating to 35 USC 112(1) rejections in the appeal brief. The examiner is of the opinion that the statements contained in the Second Declaration (paper #10), which are based solely on the opinion of the inventor, go far beyond what a skilled artisan would necessarily know or assume about the operation of the claimed invention. The declaration also provides no quantitative measure of the amount of effort that, in the opinion of the inventor, would be required by a skilled artisan to realize such claimed features. (i.e. without undue experimentation) The examiner has also asserted that the Second Declaration (paper #10) is in variance with the Inventor's previously filed declaration (paper #5). (Please see paper #11)

Appellants are further attempting to argue that disclosing detailed algorithms or techniques relating certain features (i.e. tying the generator, snooper etc. to a particular circuit or simulation) could reduce the utility of the invention as reasoning for the specifications use of broad and general terminology. However, the necessary teachings (techniques) relating to specifically how the claimed invention realizes these features were clearly disclosed in the First Declaration submitted by the appellants. (see paper 5, pages 47, exhibit A) **The examiner believes that this further buttress the examiners position and further supports the 112(1) rejections.**

The examiner is of the opinion that the specification for the claimed invention reads like a "wish list" of features, which are described in very broad and general terms, but does not contain a sufficient teaching of the claimed limitations that would allow one skilled in the art to make and/or use the invention without undue experimentation.

It is further noted that appellant's arguments regarding prior art have essentially only recited the prior art teaching followed by a recitation of the claims without pointing out the patentable distinction between the claimed invention and the prior art, or have been addressed to limitations that have not been specifically claimed.

(7) Grouping of Claims

The appellant's statement in the brief that certain claims do not stand or fall together is not agreed with because appellants have never argued (and still have not argued) the claims other than as a single group. Further, appellants have not presented any rational or explanation for their grouping in the sections entitled "grouping of

Claims" or in "Arguments". In the "Arguments" section, appellants have essentially only recited the prior art teaching followed by a recitation of the claim limitations without pointing out the patentable distinction between the claimed invention and the prior art. Therefore, the examiner considers the claims as a single group.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of prior art of record relied upon the rejection of claims under appeal.

U.S. 6,006,024	Guruswamy et al	11-1996
U.S. 6,182,258	Hollander	02-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

These rejections are set forth in prior Office Action, Paper No. 7.

Claims 1-23 stand rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which is not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Specifically, regarding independent claim 1: Claim 1 is drawn to a system for providing simulation of an integrated circuit consisting of:

*A **snooper** coupled with **the interface** for obtaining an **output** by the island.*

*A **checker** coupled with **the interface** for checking whether output is **desired output**.*

*A **generator** coupled with **the island** for providing an **input** to the island.*

*The specification of the claimed invention does not adequately disclose the operation of the claimed "**snooper**" or "**the interface**" in a way that would allow one skilled to art to make and/or use it. The specification makes reference to the snooper being "coupled with an interface" and being for "obtaining an output provided by the island during simulation and forwarding the information to the checker" but does not disclose an algorithm or technique for the implementation of either the "snooper" or "the interface".*

When "snoopers" are used in electronic systems, they are generally realized in either hardware or software. For example, software "snoopers" are can be employed by the resource manager of a communication network for purposes such as the extraction and verification of information relating to ID packets. Hardware "snoopers" are generally comprised of control logic, address sequencer, data sequencer, timing signals, and latch-and-hold circuits, and perform a similar function but are typically used for monitoring and verifying hardware status.

If the claimed "snooper" is realized in software, then an algorithm and flow chart of the "snooping" process should be disclosed. If the "snooper" is realized in hardware then a block diagram and hardware description should be provided.

The specifics of the claimed "interface" is also not disclosed in the specification. While numerous industry standard electronic interfaces such as RS-232, IEEE-488,

VME, etc. do exist, the applicants have not identified a standard interface nor have they disclosed their own design. The specifics of the claimed "interface" appear to be critical matter relating to the operation of the claimed invention and needs to be disclosed in detail.

The claimed "checker" is further not disclosed by the specification in a way that would allow one skilled in the art to make and/or use it. The specification references the checker being "coupled with the interface" and that it is for "checking the outputs to determine whether the outputs are desired outputs" but does not disclose how the checker performs the claimed "checking" of the output and does not disclose what constitutes a "desired output".

The claimed "generator" is also not disclosed by the specification in a way that would allow one skilled in the art to make and/or use it. Reference is made to the "generator" and being "coupled with an interface for providing inputs or outputs to the island" and usually "directed by a test case, but no description of the interface coupling or the related inputs and outputs is provided. Further, no description or explanation of how the generator is "directed by a test case" is given and there is no description of how the generator actually functions.

Dependent claims 2-9 inherit these defects.

Regarding independent claim 10: Claim 10 is drawn to a method for providing simulation of an integrated circuit consisting of the steps of:

***Snooping** the **interface** to obtain an output by the island.*

***Checking** the output to determine whether the **output is desired**.*

Providing *an input to the island during simulation.*

Directing *the providing of the input using a* ***test case.***

*As previously described the specification of the claimed "**snooper**", "**interface**", "**checker**", "**generator**", "**test case direction**", or the related **steps** involved in each process (i.e. "snooping", "checking" etc.) in a way that would allow one skilled to art to make and/or use it. Accordingly, independent claim 10 is rejected as described above.*

Dependent claims 11-16 inherit these defects.

Regarding independent claim 17 and dependent claims 18-23: Claims 17-23 are directed toward the computer readable medium and program instructions for the features outlined in claims 1-16 and are rejected using the reasoning as disclosed above.

Claims 1-23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,182,258 issued to Hollander in view of U.S. Patent 6,006,024 issued to Guruswamy et al.

While the specification regarding the claimed invention is delinquent in the areas cited in the 35 U.S.C. 112(1) rejections section of this office action the examiner has made prior art rejections based on the limited scope of information contained in the specification for supporting the limitations of the claims.

Independent claim 1 is drawn to a system for providing ***simulation*** *of an* ***integrated circuit*** *consisting of:*
A ***snooper*** *coupled with* ***the interface*** *monitoring island* ***output****.*

*A **checker** coupled with **the interface** for checking whether output is **desired output**.*
*A **generator** coupled with **the island** for providing an **input** to the island.*
*A **test case** directing generator to determine output based on input, intelligence to provide input based on request, generator performs particular simulation.*

*Regarding independent claims 1, 10, and 17: Hollander teaches a system, method, and computer code for functionally verifying an integrated circuit design that monitors (i.e. **snoops**) the **simulation** of an **integrated circuit** design via a **checker** (with an **interface**) and including a **test generator** **using a** **test case** **which includes** **automation** (i.e. **intelligence** for directing test) for determining the defective behavior (for **desired output**) of the circuit in a semiconductor. (Abstract, Summary of Invention, CL3-L37, CL4-L66-CL5-L7, CL8-L30, CL10-L21, Figs. 1-5)*

In the abstract Hollander recites:
"The invention is platform and simulator-independent, and is adapted for integration with Verilog, VHDL, and C functions. A modular system environment ensures interaction with any simulator through a unified **system interface** that supports multiple external types. A **test generator** module automatically creates **verification tests** from a functional description. A test suite can include any **combination of statically and dynamically-generated tests.** Directed generation constrains generated tests to specific functionalities. Test parameters are varied at any point during generation and random stability is supported. A **checking module** can perform any combination of static and dynamic checks."

*Hollander does not explicitly teach verification (testing) a substrate incorporating cells via an **island**.*

*Guruswamy teaches a **cell layout generation** system environment that includes **islands** for an integrated circuit design. (Abstract, Detailed Description, CL9-L29, CL50-L30-65, Figs. 1-5, 60-67)*

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teaching of Hollander relating to a system for

*functionally verifying an integrated circuit design that monitors (**snoops**) the **simulation** of an **integrated circuit** design via a **checker** and including a **test generator** **using a test case**, with the teachings of Guruswamy relating to a **cell layout generation** system environment that includes **islands** for an integrated circuit design to realize the claimed method for self-checking in an ASIC design. From a motivational standpoint, it further would have been obvious to apply the well known integrated circuit hardware verification techniques (i.e. "monitor (snooper)", "generator", "interface, and "checker") as taught by Hollander and simply include an **interface** to the **island** of an ASIC design to provide test case input and output data during simulation.*

*Regarding dependent claims 2-9, 11-16, 18-23: Hollander teaches a system where the **checker** incorporates an **interface** (**coupled**) to monitor (i.e. **snooper**) and **automatic test generator** for use in **integrated circuit** design where the generator and checker are obviously **reusable**. Hollander also teaches that the use a **test case** in monitoring the operation of an integrated circuit simulation. (Abstract, Summary of Invention, CL3-L37, CL4-L66-CL5-L7, CL8-L30, CL10-L21, Figs. 1-5)*

(11) Response to Argument

Regarding 35 USC 112(1) rejections: Appellants argue that examiner has failed to explain why the specification fails to describe the subject matter of the claims. The examiner asserts that the previous office action clearly defined the specific delinquencies of the specification and lack of support for the limitations of the claims on page 2, line 5-17, and page 3, line 5 to page 4, line 9. For example, regarding

enablement for the claimed "snooper", on page 3, line 5 of the previous office action the examiner stated the following:

> *"The specification of the claimed invention does not adequately disclose the operation of the claimed "**snooper**" or "**the interface**" in a way that would allow one skilled to art to make and/or use it. The specification makes reference to the snooper being "coupled with an interface" and being for "obtaining an output provided by the island during simulation and forwarding the information to the checker" but does not disclose an algorithm or technique for the implementation of either the "snooper" or "the interface".*
>
> *When "snoopers" are used in electronic systems, they are generally realized in either hardware or software. For example, software "snoopers" are can be employed by the resource manager of a communication network for purposes such as the extraction and verification of information relating to ID packets. Hardware "snoopers" are generally comprised of control logic, address sequencer, data sequencer, timing signals, and latch-and-hold circuits, and perform a similar function but are typically used for monitoring and verifying hardware status.*
>
> *If the claimed "snooper" is realized in software, then an algorithm and flow chart of the "snooping" process should be disclosed. If the "snooper" is realized in hardware then a block diagram and hardware description should be provided."*

Appellants also argue that claimed limitations relating to the interface, snooper, checker, and generator are sufficiently described in the specification to allow one skilled the art to make and/or use the invention.

As previously noted the appellants rely on statements made based on the opinion of the inventor contained in a Second Declaration (paper # 10) to support arguments relating to 35 USC 112(1) rejections in the appeal brief. The examiner asserts that the statements contained in the Second Declaration (paper #10), which are based solely on the opinion of the inventor, go far beyond what a skilled artisan would necessarily know or assume about the operation of the claimed invention. ***The examiner believes that the declarations are an attempt to cure the deficiencies of the specification and further buttress the examiners position and further supports the 112(1) rejections.***

*Regarding enablement of the term **interface**: Appellants argue that one skilled in the art would understand that interfaces include conventional I/O ports and accompanying processes for a simulated circuit and are already present in the integrated circuits of prior art. The examiner asserts that one skilled in the art would be at odds to determine how to realize the accompanying processes in support of the interfaces conventional I/O ports. The specification contains no specifics on the accompanying processes and no sufficient description of the I/O ports for a circuit being checked on a test bench and a process for controlling the I/O ports in a system clock domain. Nether the specification nor Figure 7A remedies this deficiency.*

*Regarding enablement of the term **snooper**: Appellants argue that the snooper operation is dependent on the specific IC simulation and that according to the Second Declaration one skilled in the art would realize that the snooper would include a physical portion and a logical portion in implementing the "intelligence" referenced in the specification. The examiner asserts that, while the operation of the snooper may be dependent on a specific IC and simulation, there is no sufficient disclosure of the snoopers physical portion and a logical portion for any specific or generalized case that would allow one skilled in the art to make and/or use the invention. Further, the "intelligence" required is unknown since operation of the physical portion and a logical portion are not disclosed.*

*Regarding enablement of the term **checker**: Appellants again argue that the checker operation is dependent on the specific IC simulation and that according to the Second Declaration one skilled in the art would realize that the snooper would include a*

physical portion and a logical portion in implementing the "intelligence" referenced in the specification. The examiner again asserts that, while the operation of the checker may be dependent on a specific IC and simulation, there is no sufficient disclosure of the checkers operation for any specific or generalized case that would allow one skilled in the art to make and/or use the invention. Further, the "intelligence" required is unknown since the specific interaction between the checker and snooper or messages over its interface are disclosed. Neither the specification nor Figure 7B provide sufficient teaching overcome this deficiently.

*Regarding enablement of the term **generator**: Appellants argue the generator is used to control the functions of the generator that according to the Second Declaration one skilled in the art would realize the intelligence of the generator can be viewed as providing internal data structures and a process for manipulating data structures in response to service requests. The examiner asserts that neither the specification nor Figure 7C specifically discloses how the argued control of functions or processes for manipulating data structures in response to service requests operate sufficient to allow one skilled it art the make and/or use the invention.*

*Appellants also argue that the generator generates inputs that are provided to the island, thereby simulating a device attached to the island. The examiner asserts that neither the specification nor Figure 7C specifically disclose how the invention would **simulate a device** attached to the island by inputs generated from the generator sufficient to allow one skilled in the art to make and/or use the invention.*

Accordingly, the examiner has maintained the 112(1) rejections.

The examiner also notes that Appellants have argued that the claimed limitations relating to the operation of the interface, snooper, checker, and generator are "simple" and known to one skilled in the art, and that the invention uses conventional test cases and conventional models in generating test cases to the island. This reasoning puzzles the examiner, since Appellants, in response to 112(1) rejection, appear to have essentially argued that all of the limitations of the independent claims are well-known to one of ordinary skill in the art.

Regarding 35 USC 103(a) rejections: Appellants appear to argue that Hollander both teaches synchronizing (dynamic checking) the checking model (page 7, line 1), does not teach synchronizing the checking module (page 7, lines 3-5). This argument does not make sense. In either case, the features upon which appellant relies (i.e. synchronization) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellants further argue that Guruswamy does not teach checking the behavior of a circuit. While again, checking of a circuits behavior is not recited in the language of the claims, the 35 USC 103(a) rejection from the prior office action stated the following:

"Hollander teaches a system, method, and computer code for functionally verifying an integrated circuit design that monitors (i.e. ***snoops****) the* ***simulation*** *of an* ***integrated circuit*** *design via a* ***checker*** *(with an* ***interface****) and including a* ***test generator*** *using a* ***test case*** *which includes* ***automation*** *(i.e.* ***intelligence*** *for directing test) for determining the defective* ***behavior*** *(for* ***desired output****) of the circuit in a semiconductor. (Abstract, Summary of Invention, CL3-L37, CL4-L66-CL5-L7, CL8-L30, CL10-L21, Figs. 1-5)*

In the abstract Hollander recites:

"The invention is platform and simulator-independent, and is adapted for integration with Verilog, VHDL, and C functions. A modular system environment ensures interaction with any simulator through a unified **system interface** that supports multiple external types. A **test generator** module automatically

creates **verification tests** from a functional description. A test suite can include any **combination of statically**
and dynamically-generated tests. Directed generation constrains generated tests to specific functionalities. Test parameters are varied at any point during generation and random stability is supported. A **checking module** can perform any combination of static and dynamic checks."

*Hollander does not explicitly teach verification (testing) a substrate incorporating cells via an **island**.*

*Guruswamy teaches a **cell layout generation** system environment that includes **islands** for an integrated circuit design. (Abstract, Detailed Description, CL9-L29, CL50-L30-65, Figs. 1-5, 60-67)*

*It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teaching of Hollander relating to a system for functionally verifying an integrated circuit design that monitors (**snoops**) the **simulation** of an **integrated circuit** design via a **checker** and including a **test generator using a test case**, with the teachings of Guruswamy relating to a **cell layout generation** system environment that includes **islands** for an integrated circuit design to realize the claimed method for self-checking in an ASIC design. From a motivational standpoint, it further would have been obvious to apply the well known integrated circuit hardware verification techniques (i.e. "monitor (snooper)", "generator", "interface, and "checker") as taught by Hollander and simply include an **interface** to the **island** of an ASIC design to provide test case input and output data during simulation."*

Accordingly, determining a circuits behavior is taught by Hollander as cited above. (a behavior model is also disclosed by Guruswamy at CL2-L14) Checking and generating the test outputs to the island based upon inputs is obvious by modifying Hollander in view the teachings of Guruswamy as cited above. Appellants have merely engaged in piecemeal analysis and have not clearly pointed out the patentable novelty of the claims in view of the prior art. Accordingly, the examiner has maintained the 103(a) rejection.

For the above reasons it is believed that the rejections should be sustained.

Respectfully submitted,
Fred O. Ferris III
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